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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,458	02/10/2005	Thomas Franciscus Waayers	NL02 0749 US	6330

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EXAMINER	
LE, TOAN M	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/524,458	WAAYERS, THOMAS FRANCISCUS	
	Examiner	Art Unit	
	Toan M. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11 and 12* is/are rejected.

7)☒ Claim(s) *4-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3 and 11-12 are rejected under 35 U.S.C. 102(a) as being anticipated by "Testing and Programming Flash Memories on Assemblies During High Volume Production", de Jong et al. (referred hereafter de Jong et al.).

Referring to claim 1, de Jong et al. disclose a module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin and an output pin (figure 8: "TAP"; figure 9: "PIN");

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin (figure 9; page 477, 2nd col., 2nd paragraph); and

a second register coupled to the first register for capturing the bit pattern responsive to an update signal (figure 9; page 477, 2nd col., 2nd paragraph);

characterized in that the test controller further comprises dedicated control circuitry for blocking the update signal responsive to the bit pattern (page 477-478, Dedicated Fast Flash Controller section; figure 8).

As to claim 2, de Jong et al. disclose a module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, characterized in that the dedicated control circuitry comprises a first logic gate having:

a first input for receiving the update signal;

a second input coupled to the first register for receiving the bit pattern; and

an output coupled to the second register (figure 9; page 477, 2nd col., 2nd paragraph).

Referring to claim 3, de Jong et al. disclose a module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, characterized in that the dedicated control circuitry further comprises a plurality of logic gates coupled between the first register and the second input of the first logic gate for providing the second input with the bit pattern in a modified form (page 477, 2nd col., 1st paragraph).

As to claim 11, de Jong et al. disclose an electronic device comprising a plurality of modules being substantially serially interconnected in an evaluation mode through respective input pins and output pins, a module from the plurality of interconnected modules comprising a functional block and a test controller for controlling the functional block in the evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin from the respective input pins and an output pin from the respective output pins (figure 8: "TAP"; figure 9: "PIN");

a first register coupled between the input pin and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin (figure 9; page 477, 2nd col., 2nd paragraph); and

a second register coupled to the first register for capturing the bit pattern responsive to an update signal (figure 9; page 477, 2nd col., 2nd paragraph);

characterized in that the test controller further comprises dedicated control circuitry for blocking the update signal responsive to the bit pattern (pages 477-478, Dedicated Fast Flash Controller section; figure 8).

Referring to claim 12, de Jong et al. disclose an evaluation tool comprising a set of bit patterns for evaluating an electronic device as claimed in claim 11 by providing the electronic device with the set of bit patterns, characterized in that the set of bit patterns comprises a bit pattern for triggering the control circuitry to block the update signal responsive to the bit pattern (page 477, 2nd col., 1st paragraph).

Allowable Subject Matter

Claims 4-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of claim 4 is the inclusion of a no-updated bypass register coupled between the input pin and the second input of the multiplexer.

The reason for allowance of claims 5-6 is they depend on allowable claim 4.

The reason for allowance of claim 7 is the inclusion of a further multiplexer, a first further register, a second further register, and a conductor coupled between the input pin and the second input of the further multiplexer.

The reason for allowance of claims 8-10 is they depend on allowable claim 7.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"The Algorithm of Inserting Boundary-Scan Circuit Automatically", Zhu et al., 1998 IEEE, Pages 527-531.

"Combining IEEE Standard 1149.1 With Reduced-Pin-Count Component Test", Oakland, S., 1991 IEEE VLSI Test Symposium, Pages 78-84.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Toan Le

November 14, 2006

BRYAN BUI
PRIMARY EXAMINER